WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming a gate insulating film over a semiconductor wafer;

(b) depositing a gate electrode forming film having an SiGe layer over the gate insulating film;

(c) forming at least one electrode having the SiGe layer by patterning the gate electrode forming film; and

(d) after the step (c), subjecting the semiconductor wafer to a plasma processing in an atmosphere of a mixed gas of a first gas less reactive to Ge as compared with oxygen gas and a second gas having a function of etching Si.

2. A method of fabricating the semiconductor integrated circuit device according to Claim 1, wherein the first gas is an inert gas.

3. A method of fabricating a semiconductor integrated circuit device according to Claim 2, wherein the first gas is argon gas.

4. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein the first gas is nitrogen gas.

5. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein the second gas is a gas including fluorine.

6. A method of fabricating a semiconductor integrated circuit device according to Claim 5, wherein the gas including fluorine is CHF_3.

7. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a concentration of the first gas is relatively higher than a concentration of the second gas.

8. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a concentration of Ge of the SiGe layer is equal to or larger than 10% of a total thereof.

9. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a concentration of Ge of the SiGe layer is equal to or larger than 20% of a total thereof.

10. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a concentration of Ge of the SiGe layer is equal to or larger than 40% of a total thereof.

11. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a side etching amount at two side faces of the at least one gate electrode, after the step (d), is equal to or smaller than 40% of a length, in a channel length direction, at a portion of the gate electrode forming film left after the step (c) other than the SiGe layer.

12. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein a length in a channel length direction at the SiGe layer of the at least one gate electrode, after the step (d), is equal to a length in the channel length direction at a portion of the at least one gate electrode after the step (d) other than the SiGe layer.

13. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein at least two gate electrodes are formed in the step (c), and wherein a field effect transistor of an n-channel type and a field effect transistor of a p-channel type having the gate electrodes are formed at the semiconductor wafer.

14. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein the semiconductor wafer after the step (c) is transferred to the step (d) in a state of maintaining a vacuum state.

15. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein the step (b) includes a step of introducing boron to the gate electrode forming film.

16. A method of fabricating a semiconductor integrated circuit device according to Claim 1, wherein the step (b) includes a step of depositing a silicon layer over the SiGe layer, and, after the step (d), the method further comprises the

steps of:

(e) forming side wall insulating films at side faces of the at least one gate electrode;

(f) exposing an upper face of the at least one gate electrode and portions of a main face of the semiconductor wafer;

(g) depositing a metal film having a high melting point over the semiconductor wafer; and

(h) forming a metal silicide layer having a high melting point at the upper face of the gate electrode and the portions of the main face of the semiconductor wafer.

17. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming a gate insulating film over a main face of a semiconductor wafer;

(b) depositing a gate electrode forming film over the gate insulating film;

(c) forming a gate electrode by patterning the gate electrode forming film; and

(d) after the step (c), subjecting the semiconductor wafer to a plasma processing in an atmosphere of a mixed gas of a first gas less reactive to Ge as compared with oxygen gas and a second gas having a function of etching Si,

wherein step (b) comprises the substeps of:

(i) depositing an SiGe layer; and

(ii) depositing a silicon layer over the SiGe layer.

18. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein the first gas is an inert gas.

19. A method of fabricating a semiconductor integrated circuit device according to Claim 18, wherein the inert gas is argon gas.

20. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein the first gas is nitrogen gas.

21. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein the second gas is a gas including fluorine.

22. A method of fabricating a semiconductor integrated circuit device according to Claim 21, wherein the gas including fluorine is CHF_3.

23. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein a concentration of Ge of the SiGe layer is equal to or larger than 10% of a total thereof.

24. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein a side etching amount at two side faces of the gate electrode, after the step (d), is equal to or smaller than 40% of a length in a channel length direction of the silicon layer left after the step (c).

25. A method of fabricating a semiconductor integrated circuit device according to Claim 17, wherein after the step (d), further comprising the steps of:

(e) forming side wall insulating films at side faces of the gate electrode;

(f) exposing an upper face of the gate electrode and portions of a main face of the semiconductor wafer;

(g) depositing a metal film having a high melting point over the semiconductor wafer; and

(h) forming a metal silicide layer having a high melting point at the upper face of the gate electrode and the portions of the main face of the semiconductor wafer.

26. A method of fabricating a semiconductor integrated circuit device according to claim 17, further comprising the steps of:

after the step (d), introducing a first impurity to an area for forming a field effect transistor of an n-channel type in the semiconductor wafer; and

after the step (d), introducing a second impurity, for forming a semiconductor area of a conductivity type opposite to a conductivity type of a semiconductor area formed by a first impurity, to an area for forming a field effect transistor of a p-channel type in the semiconductor wafer.

27. A method of fabricating a semiconductor integrated circuit device, comprising the steps of:

(a) forming a gate insulating film over a main face of the semiconductor wafer;

(b) depositing a gate electrode forming film over the gate insulating film;

(c) forming a gate electrode by patterning the gate electrode forming film; and

(d) after the step (c), subjecting the semiconductor wafer to a plasma processing in an atmosphere of a mixed gas of a first gas less reactive to Ge as compared with oxygen gas and a second gas having a function of etching Si, and

wherein step (b) comprises the substeps of:

(i) depositing an SiGe layer; and

(ii) depositing a metal layer over the SiGe layer.

28. A method of fabricating a semiconductor integrated circuit device according to Claim 27, wherein a side etching amount at two side faces of the gate electrode after the step (d) is equal to or smaller than 40% of a length in a channel length direction of the metal layer after the step (c).

29. A method of fabricating a semiconductor integrated circuit device according to Claim 27, wherein the step (b) includes a step of depositing the metal layer after introducing boron to the SiGe layer.